W VLSI Design Roadmap with Timeline

Week 1: Introduction to VLSI

- Understand what VLSI means and why it is important.
- Study Moore's Law and the evolution of IC design.
- Explore real-world applications: microprocessors, memory, ASICs, SoCs.

Week 2: Basic MOS Transistor Theory

- Learn the structure and operation of MOSFETs (nMOS, pMOS).
- Study threshold voltage, channel formation, and I-V characteristics.
- Introduction to SPICE models.

Week 3: CMOS Technology

- CMOS inverter design and its characteristics.
- Explore static and dynamic behavior of CMOS.
- Study power consumption (static vs dynamic power).

Week 4: Fabrication Process

- Wafer preparation and oxidation.
- Photolithography, etching, ion implantation.
- Metallization and packaging.

III Week 5: VLSI Design Flow

- Complete flow: Specification \rightarrow RTL \rightarrow Simulation \rightarrow Synthesis \rightarrow Layout \rightarrow Fabrication.
- Understand HDL languages (VHDL/Verilog) and RTL modeling.
- Introduction to simulation and testbenches.

III Week 6: Combinational Logic Design

- Logic gates and Boolean algebra.
- Multiplexers, Encoders, Decoders, Adders.
- Gate-level and dataflow modeling in Verilog.

III Week 7: Sequential Logic Design

- Latches and Flip-Flops.
- Counters, Registers, and Finite State Machines (FSM).
- Design and simulate sequential circuits.

III Week 8: Timing Analysis and Optimization

- Setup time, hold time, and propagation delay.
- Timing violations and mitigation.
- Clock skew and jitter concepts.

III Week 9: Layout Design and EDA Tools

- Floorplanning, placement, and routing.
- Stick diagrams and layout rules.
- Tools: Cadence, Synopsys, Xilinx (overview).

Week 10: Testing and Verification

- Fault models: stuck-at, bridging faults.
- Automatic Test Pattern Generation (ATPG).
- Design for Testability (DFT): Scan chains, BIST.

III Week 11: Low Power VLSI Design

- Techniques to reduce power: Clock gating, Multi-Vt, Power gating.
- Dynamic Voltage and Frequency Scaling (DVFS).
- Low power design considerations during RTL and layout.

💷 Week 12: Project / Case Study

- Design a small processor or digital system.
- RTL simulation, synthesis, and layout (basic level).
- Document the process and present the project.